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(54) **VHF/UHF plasma process for use in forming integrated circuit structures on semiconductor wafers.**

(57) A method of fabricating integrated circuit structures on semiconductor wafers using a plasma-assisted process is disclosed wherein the plasma is generated by a VHF/UHF power source at a frequency ranging from about 50 to about 800 MHz. Low pressure plasma-assisted etching or deposition processes, i.e., processes may be carried out within a pressure range not exceeding about 500 milliTorr; with a ratio of anode to cathode area of from about 2:1 to about 20:1, and an electrode spacing of from about 5 cm. to about 30 cm. High pressure plasma-assisted etching or deposition processes, i.e., processes may be carried out with a pressure ranging from over 500 milliTorr up to 50 Torr or higher; with an anod to cathode electrod spacing of less than about 5 cm. By carrying out plasma-assisted processes using plasma operated within a range of from about 50 to about 800 MHz, the electrode sheath voltages are maintained sufficiently low, so as to avoid damage to structures on the wafer, yet sufficiently high to preferably permit initiation of the processes without the need for supplemental power sources. Operating in this frequency range may also result in reduction or elimination of microloading effects.

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This invention relat s to the processing of semiconductor wafers to form integrated circuit structures thereon.

In the processing of semiconductor wafers to form integrated circuit structures thereon, plasma-assisted processes are often utilized either in deposition, or etching process steps. In such processes, e.g., reactive ion etching (RIE), plasma etching, CVD facet, or conformal isotropic CVD, radio frequ ncy power from a generator or power source is generally applied to electrodes within a vacuum processing chamber via a matching network of some kind which will maximize the power transfer from the generator or power source to the plasma. When an electric field of sufficient magnitude is established between electrodes in the vacuum chamber, the field accelerates electrons present in the gas which undergo collisions with gas molecules. Very little energy can be transferred through elastic processes, because of the large mass difference between electrons and atoms or molecules, so the electron gains energy from the field and eventually may collide inelastically with a gas molecule, exciting or ionizing it. Ionization can liberate additional electrons, which are, in turn, accelerated by the field. The process avalanches, causing gas breakdown, resulting in a steady state plasma when ionization and recombination processes are balanced. Highly reactive ions and radical species are produced which are used to etch or deposit materials on semiconductor wafers.

The power sources used for such prior art generation of plasmas conventionally utilized electromagnetic radiation at low frequencies ranging from about 10-400 kHz, at high frequencies ranging from about 13 to about 40 MHz (typically at 13.56 MHz), and at microwave frequencies ranging from about 900 MHz up to 2.5 GHz.

At low frequencies of 10-400 kHz, both ions and electrons can be accelerated by the oscillating electric field, as well as any steady state electric field or bias developed in the plasma, resulting in the risk of potential damage to sensitive devices being fabricated on the wafer. At higher frequencies of 13-40 MHz, the so-called high frequency range, steady state electrode sheath voltages may be developed ranging from several hundred to over 1000 volts. This creates a problem since device damage is a concern at voltages exceeding about 200 volts, depending upon the device structure, material, and other factors.

The problem of high sheath voltage has been ameliorated by the use of microwave power sources to excite the plasma, i.e., power sources at a frequ ncy range of from about 900 to about 2.5 gHz. Such techniques produce a plasma at low particle energies, i.e., 10-30 v. Howev r, the use of microwave frequencies can result in loss of anisotropy (vertical natur) of the tch, apparently due to the lowering of the sheath voltage; and can slow the etch or deposition rate down, apparently due to lowering of the particle energy level. In fact, in some cases the threshold energy level for certain processes, e.g., reactive ion etching of SiO_2, cannot be reached using only microwave energy to power the plasma.

Because of such shortcomings in the use of a purely microwave energy source, microwave energy has been used in combination with another power source at high frequency, e.g. 13.56 MHz, to raise the sheath voltage at the wafer sufficiently to achieve the desired anisotropy in the etch. Microwave ECR sources use a microwave source and a magnetic field such that the ECR condition is met, that is, the radian frequency of the microwave source $w = |B|e/m$ where $|B|$ is the magnetic field magnitude and e and m are the electron charge and mass respectively. This produces a high density, low energy plasma at low pressures. A divergent magnetic field can be used to extract ions and accelerate them to higher energies, and/or a high frequency bias may be applied to the wafer to increase ion energy.

However, such usage and coordination of multiple power source systems further complicates the apparatus used in carrying out such etching and/or deposition processes. Furthermore, the use of an ECR system necessitates the use of lower operating pressures ranging, for example, from 0.1 to several milliTorr. *This, in turn, results in a reduction in the maximum flow rate of etching or deposition gases through the reaction chamber unless a very large vacuum pump is used.

It would, therefore, be desirable to conduct plasma-assisted processes using a power source wherein sheath voltages could be developed low enough to avoid risk of damage to devices on the wafer, yet high enough to achieve desired anisotropy, and at reaction rates comparable to prior art processes.

This object is solved by the processes of independent claims 1, 5, 18, 29 and 41. Further advantageous features, aspects and details of the invention are evident from the dependent claims, the description and the drawings. The claims are intended to be understood as a first non-limiting approach of defining the invention in general terms.

The invention therefore relates to the use of a VHF/UHF plasma in the processing of semiconductor wafers, i.e., a VHF/UHF plasma process for use in forming integrated circuit structures on semiconductor wafers.

*1 milliTorr= 1.3x10* bar

It is, ther fore, an aspect of the invention to provide plasma-assisted processing for the production of integrated circuit devices on semiconductor wafers using a power source having a fraquency range of from about 50 MHz up to about 800 MHz.

It is another aspect of the invention to provide a plasma-assisted RIE process for etching materials used in the fabrication of integrated circuit devices on semiconductor waters which comprises using a powar source having a frequency range of from about 50 MHz up to about 800 MHz and maintained at a power density level ranging from about 10 to about 76 watts/inch^2 *of wafer area in a vacuum chamber at a pressure within a range of from about 2 to about 500 milliTorr.

It is yet another aspect of the invention to provide a plasma-assisted RIE process for etching sillcon oxlde on semiconductor waters which comprises using a powar source having a fraquency range of from about 100 MHz up to about 250 MHz and maintalned et a power denslty level ranglng trom about 30 to about 76 watts/inch^2 of wafer area In a vacuum chamber at a pressure within a range of from about 2 to about 500 milliTorr, while flowing one or more etching gases and an optional inert gas through the chamber, with an effective area ratio of anode to cathode of at least about 2:1 and an electrode spacing of 5 cm. or more, to provide an anisotropic etch with an atch rate of from about 0.3 to 0.75 µm/minute.

It Is still another aspect of the invention to provide a plasma-assisted RIE process for anIsotropically etching silicon oxlde on semlconductor wafers which comprises using a power source having a frequency range of from about 100 MHz up to about 250 MHz and maintained at a power density level ranging trom about 45 to about 56 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from about 20 to about 200 milliTorr, while flowing a source of fluorine, an optional sourca of hydrogen, a source of carbon, and an optional inert gas through the chamber, with an effective area ratio of anode to cathode of from about 2:1 to about 20:1, and an electrode spacing of from about 5 cm to about 30 cm , to provide an anisotropic etch with an etch rate of from about 0.3 to about 0.75 µm par minute.

It is a further aspect of the invention to provide a plasma-assisted RIE process for selectively anisotropically etching silicon oxide on semiconductor wafers, with respect to polysilicon or photoresist, which comprises using a power source having a frequancy ranga of from about 100 MHz up to about 250 MHz and maintained at a power density level ranging from about 45 to about 56 watts/inch^2 of wafer area in a vacuum chamber at a prassure within a rang of from about 20 to about 200 milliTorr, while flowing a source of fluorine, an optional source of hydrogen, a source of carbon, and an optional inert gas through tha chamber, wherein the atomic ratio of carbon to fluorine ranges from about 0.1:1 to about 2:1 and the atomic ratio of hydrogan (when present) to fluorine ranges from about 0.1:1 to about 0.5:1, with an effective area ratio of anode to cathode of from about 2:1 to about 20:1, and an electrode spacing of trom about 5 cm to about 30 cm , to obtain a ratio of silicon oxide etch (thickness) rate to polysilicon or photorasist atch (thicknass) rate of from about 2:1 to over 30:1, with an etch rate of from about 0.3 to about 0.75 µm per minute.

It is yet a further aspect of the invention to provide a plasma-assisted RIE process for etching polysillcon and/or aluminum on semiconductor wafers which comprises using a power source having a frequency range ot from about 100 MHz up to about 800 MHz and maintained at a power denslty level ranging from about 10 to about 76 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of trom about 2 to about 500 milliTorr, while flowing one or more etching gases and an optional Inert gas through tha chamber, wlth a ratio of anode to cathode area of at least about 2:1 and an electrode spacing of 5 cm. or more, to provide an anisotropic etch with an etch rate of from about 0.2 to about 1.0 µm/minute.

It is still a further aspect of the invention to provide a plasma-assisted RIE process for anisotropically etching polysllicon and/or aluminum on semiconductor wafers which comprises using a power source having a frequency range of from about 150 MHz up to about 600 MHz and maintained at a power density level ranging trom about 20 to about 40 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from about 20 to about 200 milliTorr, while flowing a sourca of chlorine and an optional inert gas through the chamber, with a ratio of anoda to cathode area of from about 2:1 to about 20:1, and an electrode spacing of from about 5 cm to about 30 cm , to provide an anisotropic etch with an etch rate of from about 0.5 to about 0.7 µm/minute.

It is another aspect of the invantion to provide a plasma-assisted etching process for etching materials used in the fabrication of integrated circuit devices on semiconductor wafers which comprises using a power source having a frequency range of from about 50 MHz up to about 800 MHz and maintained at a power dansity level ranging from about 15 to about 76 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from ov r 500 milliTorr to about 50 Torr.

* 1 inch^2 = 6.5cm^2

It is yet anoth r aspect of the invention to provida a plasma-assisted etching process for etching silicon oxide on semiconductor wafers which comprises using e power source having a frequency ranga of from about 100 MHz up to about 200 MHz and maintained at a power density level ranging from about 30 to about 50 watts/inch^2 of wafer area in a vecuum chember et a pressure within a range of from about 1 Torr to about 20 Torr, while flowing a source of fluorine, a source of carbon, an optionel source of hydrogen, and an optional inert gas through the chamber, with an anode to cathode electrode spacing of less than ebout 5 cm., to provide an etch rete of from about 0.2 to about 1.0 µm/minute.

It is sill another aspect of the invention to provida a plasme-essisted atching process for selectively etching silicon oxide on semiconductor wafers, with respect to the etching of polysilicon or photoresist, which comprises using a power source having a frequency range of from about 100 MHz up to about 200 MHz and meintained at a power density leval ranging from about 30 to about 50 watts/inch^2 of wafar area In a vacuum chamber at a pressure within a range of from about 1 Torr to about 20 Torr, while flowing a source of fluorine, a source of carbon, an optional sourca of hydrogan, and an optional inert gas through the chamber, wherein the atomic ratio of carbon to fluorine ranges from about 0.1:1 to about 2:1 and the atomic ratlo of hydrogen (when prasent) to fluorine ranges from about 0.1:1 to about 0.5:1, with a cathode to anode electrode spacing of less than ebout 5 cm , to obtain a ratio of silicon oxide etch (thickness) rate to polysilicon or photoresist etch (thickness) rate of from about 2:1 to ovar 30:1, with an atch rate of from about 0.2 to about 1.0 µm per minute.

It is still a further aspect of tha invantion to provide a plasma-assisted etching process for etching polysilicon and/or aluminum on semiconductor wafars which comprises using a powar source having a frequency range of from about 100 MHz up to about 200 MHz and maintained at a power density level ranging from about 20 to about 40 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from about 1 Torr to ebout 20 Torr, whila flowing a source of chlorine and an optional inert gas through the chamber, with an anoda to cathode electroda spacing of less than about 5 cm , to provida an atch rate of from about 0.2 to 1 about µm/minute.

It is another aspect of the invention to provide e plasme-assistad CVD facet daposition process for depositing materials used in the fabrication of int grated circuit devices on semiconductor waf rs which comprises using a powar sourca having a frequ ncy rang of from about 50 MHz up to about 800 MHz and maintain d at a power d nsity level ranging from about 10 to about 76 wetts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from about 2 to about 500 milliTorr.

It is yet another aspect of the invention to provide a plasma-assisted CVD facet deposition process for depositing silicon oxide on semiconductor wafers which comprises using a power source having a frequency range of from about 100 MHz up to about 250 MHz and meintained at a power density level ranging from about 10 to about 76 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from about 2 to about 500 milliTorr, while flowing one or more sources of silicon, one or mora sources of oxygen, end an optionel inert ges through tha chamber, with a ratio of anode to cathode area of at least about 2:1 and an electrode spacing of 5 cm. or more, to provide a daposition rata of from about 0.1 to about 1.5 µm/minute.

It is still another aspect of the invention to provide e plasma-assistad CVD fecat daposition process for depositing silicon oxide on semiconductor wafers which comprises using a power source having a frequency range of from about 100 MHz up to about 250 MHz and maintained at a power density level ranging from about 45 to about 56 watts/inch^2 of wafer area in a vacuum chamber at a prassure within e ranga of from about 20 to about 200 milliTorr, while flowing one or more sources of silicon, one or more sourcas of oxygen, and an optional inert gas, through the chamber, with a ratio of anode to cathode area of from about 2:1 to about 20:1, and an electrode spacing of from about 5 cm to about 30 cm, to provida a deposition rata of from about 0.4 to about 1.0 µm/minute.

It is yet a further aspect of the invention to provide a plasma-assisted CVD facet deposition process for depositing silicon nitride on semiconductor wafers which comprises using a power source having a frequency range of from about 100 MHz up to about 250 MHz and maintained at a power density level ranging from about 10 to about 76 wetts/inch^2 of wefer erae in a vecuum chamber at a pressure within a range of from about 2 to about 500 milliTorr, while flowing one or more sources of silicon, one or more sourcas of nitrogen, an optional source of hydrogen, and an optional inert gas, through the chamber, with a ratio of anoda to cathode araa of at least about 2:1 and an electrode spacing of 5 cm. or more, to provide a deposition rate of from about 0.1 to about 1.5 µm/minuta.

It is still a further aspect of the invention to provid a plasma-assisted CVD facet deposition process for depositing silicon nitride on semiconductor wafers which comprises using a power

source having a frequ ncy range of from about 100 MHz up to about 250 MHz and maintained at a power density level ranging from about 45 to about 56 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from about 20 to about 200 milliTorr, while flowing one or more sources of silicon, one or more sources of nitrogen, an optional source of hydrogen, and an optional inert gas, through the chamber, with a ratio of anode to cathode area of from about 2:1 to about 20:1, and an electrode spacing of from ebout 5 cm to about 30 cm, to provide a deposition rate of from about 0.4 to about 1.0 µm/minute.

It is enother aspect of the invention to provide a plasma-assisted CVD conformal isotropic deposition process far depositing materials used in the fabrication of integrated circuit devices on semiconductor wafers which comprises using a power source having a frequency range of from about 50 MHz up to about 800 MHz and maintained at a power density level ranging from about 10 to about 38 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from over 500 milliTorr to about 50 Torr.

It is yet another aspect of the invention to provide a plasma-assisted CVD conformal isotropic deposition process or depositing silicon oxide on semiconductor wafers which comprises using a power source having a frequency range of from about 150 MHz up to about 800 MHz and maintained at a power density level ranging from ebout 10 to about 38 watts/inch^2 of wafer area in a vacuum chambar at a pressure within a range of over 500 milliTorr to about 50 Torr while flowing one or more sources of silicon, one or more sources of oxygen, and an optional Inert ges through the chember, with an anode to cathode electrode spacing of less than about 5 cm, to provide a deposition rate of from about 0.5 to about 1.0 µm/minute.

It is still another aspect of the invention to provide a plasma-assisted CVD conformal isotropic deposition process for depositing silicon oxide on semiconductor wafers which comprises using a power source having a frequency range of from about 150 MHz up to about 800 MHz and maintained at a power density level ranging from about 10 to about 38 watts/inch^2 of wefer area in e vacuum chamber at a pressure within a range of from about 1 Torr to about 20 Torr, while flowing one or more sources of silicon, one or more sources of oxygen, and an optional inert gas, through the chamber, with an anode to cathode electrode spacing of less then ebout 5 cm, to provide a deposition rate of from about 0.5 to about 1.0 µm/minut .

It is yet a further aspect of the invention to provide a plasma-assisted CVD conformal isotropic deposition process for depositing silicon nitride on semiconductor wafers which comprises using a power source having a frequency range of from about 150 MHz up to about 800 MHz and maintained at e power density level renging from about 10 to about 38 watts/inch^2 of wafer area in a vacuum chamber at a pressure within a range of from over 500 milliTorr to about 50 Torr, while flowing one or more sources of silicon, one or more sources of nitrogen, an optional source of hydrogen, and an optional inert gas, through the chamber, with an anode to cathode electrode spacing of less than about 5 cm, to provide a deposition rate of from about 0.5 to about 1.0 µm/minute.

It is still a further aspect of the invention to provide a plasma-assisted CVD conformal isotropic deposition process for depositing silicon nitride on semiconductor wafers which comprises using a power source having a frequency range of from about 150 MHz up to about 800 MHz and maintained at a power density level ranging from ebout 10 to about 38 watts/inch^2 of wafer area in e vacuum chamber at a pressure within a range of from ebout 1 Torr to about 20 Torr, while flowing one or more sources of silicon, one or more sources of nitrogen, an optionel source of hydrogen, and an optional Inert gas, through the chamber, with an anode to cathode electrode spacing of less than about 5 cm, to provide a deposition rate of from about 0.5 to about 1.0 µm/minute.

Figure 1 is e flow sheet illustrating RIE low pressure etching using the plasma-assisted process of the invention.

Figure 2 Is a flow sheet Illustrating high pressure etching using the plasma-assisted process of the invention.

Figure 3 is a flow sheet illustrating low pressure CVD (facet) deposition using the plasma-assisted process of the invention.

Figure 4 is a flow sheet illustrating high pressure CVD conformal isotropic deposition using the plasma-assisted process of the invention.

The invention provides en Improved method of fabricating integrated circuit structures on a semiconductor water mounted on a cathode and spaced from an anode in a vacuum chamber using a plasma-assisted process wherein the plasma is generated by a power source coupled to the cathode and anode in the vacuum chamber and operated at a frequency ranging from about 50 to ebout 800 MHz, which may be termed a VHF/UHF power source.

Preferably the power source generates power within a frequency range of from about 50 to about 500 MHz for low pressure plasma-assisted proc sses, i.e., process s carried out in a vacuum chamber maintained within a pressure range not xce ding about 500 milliTorr; with a ratio of anode

to cathode area of from about 2:1 to about 20:1, end en electrode spacing of from ebout 5 cm to about 30 cm.

The power source preferably generates power within e frequency renge of from ebout 100 MHz to about 800 MHz for high pressure plasma-assisted processes, i.e., processes carried out in a vacuum chember meinteined at e pressure renging from ov r 500 milliTorr up to 50 Torr or higher; with an anode to cathode electrode spacing of less than ebout 5 cm.

By carrying out plasma-assisted processes wherein the plasma is generated by a power source at e frequency within e range of from about 50 to about 800 MHz, the sheath voltages are maintained sufficiently low, so as to avoid damage to structures on the wefer, yet sufficiently high to preferably permit initiation of the processes without th need for supplemental power sources. Furthermore, the operation of e plasme within this frequency range results in e satisfactory rate of deposition and/or etch due to the decrease in ion energy and increase in ion flux density due to the respective decrease in the rf voltage component of the plesma and current increase due to the drop in plasma impedence at these frequencies. In addition, the establishment and powering of a plasma within this frequency range may result in reduction or elimination of microloading effects, e.g., the same etch rate may be maintained regardless of opening size.

The term "sheath", as used herein, denotes an electron deficient region developed et eech electrode in the plasme. The term "sheath voltage" used herein means the voltage developed across the perticular electron deficient region, i.e., the particular sheath, between the plasma end the electrode (cathode or enode).

The use of a plesme energized by a power source operated at a frequency ranging from about 50 MHz to ebout 800 MHz, in etching and/or deposition processes carried out in accordance with the invention, may be in combination with the use of auxiliary magnets arranged around the exterior of the chember for megnetic enhancement. The plasma may be coupled to more than one power source, including a power source which may be opereted outside of the frequency renge of from about 50 MHz to ebout 800 MHz.

The invention may be used in reactive ion etching (RIE) et low pressures, i.e., 500 milliTorr and lower; in plasma etching at higher pressures, i.e., pressures above 500 millitorr; in chemical vapor deposition (CVD) facet processes et low pressur , i. ., 500 milliTorr and lower; and in conformal isotropic CVD processes at higher pressures, i.e., pressures above 500 milliTorr.

The process of the inv ntion may be used in any conventional vacuum etching or deposition apparetus such as the epparetus disclosed in European patent application EP 90119065.2, cross-reference to which is hereby made. However, it is important to the practice of the process of the invention that the power source, operating in the frequency range of from about 50 MHz to about 800 MHz in accordence with the invention, be properly coupled to the vacuum chamber. A network for properly matching the power source and coupling this power to the plesme within the vacuum chamber within this frequency range is disclosed and claimed in European patent application, entitled "Plasma Processing Reector", (our file A5501-EP), filed on even date and assigned to the same assignee, which is included by reference and e copy of which is enclosed.

A. Reactive Ion Etching

In accordance with the invention, materials, such as silicon oxide, polysilicon, and aluminum mey be removed by a reective ion etch (RIE) process using a plasma coupled to e power source operating within e frequency range of 50 MHz to 800 MHz, preferably within a frequency renge of 50 MHz to 600 MHz at a pressure not exceeding about 500 milliTorr.

The ratio of total effective anode area to total effective cathode aree in an RIE process carried out in accordance with the invention (with the wafer mounted on the cathode) will preferably range from ebout 2:1 anode aree to cathode area up to about 20:1 with the everage anode to cathode electrode spacing ranging from about 5 cm to ebout 30 cm. The "effective aree" of the enode or cathode, es used herein, may be defined as the area of the electrode coupled to the plasme.

When a silicon oxide, such es, SiO_2, is to be removed, the frequency of the plasma power source will preferably be maintained within a range of from ebout 100 to ebout 250 MHz, with a typical frequency for the plasma power source maintained at from about 150 MHz to about 200 MHz. Higher frequencies can be used, up to about 800 MHz, but the etch rate and the anisotropy of the etch may be lowered thereby below acceptable limits.

The pressure used for RIE silicon oxide etching in the practice of the invention will range from about 2 milliTorr up to about 500 milliTorr, and will preferably range from about 20 to about 200 milliTorr, with a typical pressure being ebout 50 milliTorr.

The power density of the plesma used for etching silicon oxide in accordance with the invention (in watts/inch^2 of waf r area) will range from ebout 30 to ebout 76 watts/inch^2, e.g., from about

600-1500 watts for a typical 5" *diameter wafer; preferably the power density mey range from about 45 to about 56 watts/inch^2.

Various etching chemistries may be used in the practice of the RIE process of the invention for the removal of silicon oxide which will include one or more fluorine-containing gases, one or more carbon-containing gases, end optionally one or more hydrogen containing gases. Typical gases and mixtures of gases may include CF_4, C_2F_6, C_4F_8, CHF_3, CH_3F end CHF_3, CH_3F and CF_4, CHF_3 and CF_4, CF_4 and CH_4, C_2F_6 and CHF_3, C_4F_8 and CHF_3, NF_3 and CH_4, SF_6 and CH_4, CF_4 end H_2, and combinations of such geses or mixtures of gases. An optional oxygen source may be combined with any of the above mixtures to control selectivity of the etch, as is well known to those skilled in the art. An inert flow gas, such as Argon, may be optionally used with any combination of etching gases to improve the anisotropy of the etch. Flows of each of the gases used for a typical 10-15 liter etching chamber may range from about 1 to about 300 sccm, depending upon the vacuum pump size used for the desired pressure range.

RIE removal of silicon oxide, using the process of the invention, results in an oxide removal rate renging from about 0.3 to 0.75 µm/minute for an oxide grown thermally under wet oxide conditions (grown in steam). The etch is highly anisotropic in nature, with no discernible damage to the integrated circuit structures remelning on the wafer.

When it is desired to provide a silicon oxide etch which is selective to silicon oxide, with respect to polysilicon or photoresist, the atomic ratio of carbon to fluorine should range from about 0.1:1 to about 2:1; and the atomic ratio of hydrogen (when it is present in one of the gases) to fluorine should range from about 0.1:1 to about 0.5:1.

Aluminum end polysilicon mey elso be removed by an RIE process carried out in accordance with the invention using a power source operated at a frequency of from about 100 MHz to about 800 MHz, preferably from about 150 MHz to about 600 MHz.

The pressure used for the RIE removal of aluminum and/or polysilicon may be the same as that used for the RIE removal of oxide, i.e., a low pressure renging from about 2 milliTorr to about 500 milliTorr and preferably ranging from about 20 milliTorr to about 200 milliTorr.

The RIE removel of eluminum and/or polysilicon, in accordance with the process of the invention, is carried out using a plesma power density ranging from about 10 to about 76 watts/in^2 of wafer ar a, e.g., from about 200-1500 watts for a 5" diameter wafer; and pref rably a power density ranging from about 20 to about 40 watts/inch^2.

Typicel RIE chemistries useful in the removel of aluminum and/or polysilicon may be mployed in the practice of the process of the invention, such as a mixture of a chlorine-conteining ges with an inert gas; e.g., a mixture of Cl_2 and Ar, or a mixture of BCl_3 and Ar. Typical flow rates of such gases for a 10-15 liter etch chamber may also renge from about 10 to about 100 sccm for either the chlorine-containing gas or the inert gas, such as argon.

Etch removal retes for an aluminum and/or polysilicon RIE process carried out in accordance with the invention may range from about 0.2 to about 1.0 µm/minute, preferably ranging from about 0.5 to about 0.7 microns/minute. The etch is highly anisotropic in nature, with no discernible damage to the remaining integrated circuit structures on the wafer.

Single crystal silicon may also be removed using the RIE process of the invention by varying the chemistry used in etching silicon oxide, e.g., using a source of fluorine, and optional sources of carbon and oxygen.

B. Plasma-assisted High Pressure Etching

The etch removal of oxides of silicon, as well as aluminum and/or polysilicon, may also be carried out using high pressures, i.e., pressures over 500 milliTorr up to 50 Torr or higher. When such e high pressure plasma-assisted etch process is used in accordance with the invention, for removal of materials such as aluminum and/or polysilicon, the frequency of the power source used to energize the plasma will range from about 50 MHz to about 800 MHz, preferably from about 100 MHz to about 200 MHz; and the pressure will range from over 500 milliTorr to about 50 Torr or higher, preferably from ebout 1 Torr to about 20 Torr.

The power density will range from about 15 to about 76 watts/inch^2 of wafer area, preferably from about 30 to about 50 wetts/inch^2. The anode to cathode electrode will range from about 0.2 cm up to about 5 cm. so that plasma completely fills the volume between the electrodes.

Etching chemistries used in the practice of the high pressure plasma-assisted etching process of the invention for the removal of silicon oxide include one or more fluorine-containing gases, one or more carbon-containing gases, and optionally one or more hydrogen containing gases. Typical gases and mixtures of gases may include CF_4, C_2F_6, C_4F_8, CHF_3, CH_3F and CHF_3, CH_3F and CF_4, CHF_3 and CF_4, CF_4 and CH_4, C_2F_6 and CHF_3, C_4F_8 and CHF_3, NF_3 and CH_4, SF_6 and CH_4, CF_4 and H_2, and combinations of such gases or mix-

* 1 inch = 2.5 cm

tures of gases. An optional oxyg n source may b combined with any of the above mixtures to control selectivity of the etch, as is well known to those skilled in the art. An inert flow gas, such as Argon, may be optionally used with any combination of etching gases, if desired, to control the profile of the etch. Flows of each of the gases used for a typical 10-t5 liter etching chamber may range from about 1 to about 300 sccm, depending upon the vacuum pump size used for the desired pressure range.

Etch rates of such high pressure plasma-assist d etches, which are carried out in accordance with the invention, will range from about 0.2 to about 1.0 µm/minute.

The etch chemistries useful in the removal of aluminum and/or polysilicon, in the practice of the process of the invention, are the same as used in the low pressure RIE process, i.e., a mixture of a chlorine-containing gas with an inert gas; e.g., a mixture of Cl_2 and Ar, or a mixture of BCl_3 and Ar. Typical flow rates of such gases for a 10-15 liter etch chamber may also range from about 10 to about 100 sccm for either the chlorine-containing gas or the inert gas, such as argon. Etch removal rates for aluminum and/or polysilicon, using such chemistries, may range from about 0.2 to about 1.0 µm/minute.

Single crystal silicon may also be removed using the high pressure etching process of the invention by varying the chemistry used in etching silicon oxide, e.g., using a source of fluorine, and optional sources of carbon and oxygen.

C. CVD Low Pressure (Facet) Deposition

The improved method of fabricating integrated circuit structures using a plasma-assisted process, wherein the plasma is generated by a power source at a frequency ranging from about 50 to about 800 MHz, may also be used for plasma-assisted deposition processes, such as a low pressure CVD process.

In such a process, sometimes known as a CVD facet process, etching of the materials (e.g., oxide or nitride) deposited on the outside (upper) corners of a trench in the silicon wafer is also carried out simultaneously with the deposition of oxide or nitride into the trench to thereby avoid formation of voids in the filler material. In the prior art, such faceting and deposition was carried out simultaneously in ECR/microwave frequency plasma CVD, while the prior art use of plasma-assisted CVD at high frequencies, such as the popular 13.56 MHz, resulted in the ne d for cycling the waf r between a deposition chamb r and an etching chamber to achieve the desired faceting.

In accordance with the inv ntion, simultaneous low pr ssur CVD d position and fac ting may be carried out using a plasma-assisted CVD process wher in the plasma is energized by a power source operating in a frequency range of about 50 MHz to 800 MHz, and preferably in a frequency range of from about 100 MHz up to about 250 MHz. Thus, the use of complicated microwave/ECR equipment, or need for cycling the wafer between deposition and etching chambers, may be avoided by the practice of the process of the invention.

The power density of the plasma during such a plasma-assisted CVD facet deposit should be maintained in a range of from about 10 to about 76 watts/in^2, preferably from about 30 to about 76 watts/in^2, and most preferably within a range of from about 45 to about 56 watts/in^2.

The deposition rate of either oxide or nitride will vary with the power density of the plasma with a power density range of 10 to 76 watts/in^2 resulting in a deposition rate ranging from about 0.1 to about 1.5 µm/minute, while operating in the power density range of from about 45 to about 56 watts/in^2 will result in a deposition rate ranging from about 0.4 to 1.0 µm/minute until the desired thickness of the material, e.g., oxide or nitride, has been deposited.

The pressure within the deposition chamber during such a plasma-assisted CVD facet deposition should be maintained within a range of from about 2 milliTorr up to about 500 milliTorr, preferably from about 20 milliTorr up to about 200 milliTorr.

The ratio of total effective area of the anode in the deposition chamber to the total effective area of the cathode (on which the wafer is supported), where "effective area", as previously defined, is the area coupled to the plasma, will range from a minimum of about 2:1 to about 20:1; while the spacing between the anode and the cathode will be at least about 5 cm up to as much as 30 cm.

When depositing silicon oxide by this method, one or more sources of silicon and one or more sources of oxygen are flowed into the deposition chamber, as well as an optional inert gas such as Argon.

The source of silicon may be a gaseous source such as silane (SiH_4) or vapor from a liquid source such as an organic silicon source, e.g. tetraethylorthosilicate (TEOS). The source of oxygen may be O_2, N_2O, or a combination of same, either with or without a minor amount of O_3, or any other convenient source of oxygen. A dopant source may also be flowed into the reactor if it is desired to deposit a doped glass.

Typical flows of gas into a 5-10 lit r deposition chamber, using silane as the source of silicon and O_2 or N_2O as the source of oxygen, with an Argon gas, would be about 10-150 sccm of SiH_4, about

10-300 O_2 or N_2O, and from 0 to about 500 sccm Argon. If TEOS is used as the source of silicon, typical flows range from about 0.1 to about 1.0 grams/minute.

Silicon nitride may be deposited on the semiconductor wafer instead of silicon oxide under the same deposition conditions by substituting a source of nitrogen for the source of oxygen, while using any of the above noted sources of silicon that do not form an oxynitride. It should be noted, in this regard, that the so-called silicon nitride formed may not be a true Si_3N_4 compound, but rather a $Si_xH_yN_z$ compound which is, however, customarily referred to as silicon nitride, or simply "nitride".

When depositing such a silicon nitride layer, nitrogen and ammonia may be used as sources of nitrogen. An optional source of hydrogen may also be supplied. Typical gas flows for deposition of silicon nitride, under the same conditions as for the deposition of silicon oxide, would be about 10 to about 150 sccm SiH_4, about 25 to about 300 sccm N_2, about 0 to about 50 sccm NH_3, 0 to about 50 sccm hydrogen, and 0 to about 500 sccm Argon.

If it is desired to deposit silicon oxynitride on a semiconductor wafer, a source of oxygen may be additionally supplied to the reactants used in forming silicon nitride, without substantially changing any other reaction conditions.

D. High Pressure CVD (Conformal Isotropic) Deposition

Deposition of an isotropic conformal layer of materials such as silicon oxide and silicon nitride may also be made in accordance with the invention under high pressure conditions, i.e., at pressures exceeding 500 milliTorr up to as high as 50 Torr or higher, but preferably ranging from about 1 Torr to about 20 Torr, using a plasma powered by a power source at a frequency within the range of about 50 MHz up to about 800 MHz, preferably from about 150 MHz to about 800 MHz, and maintained at a power density of from about 10 to about 38 watts/in^2 of wafer area, e.g., at a power level of about 200 to about 750 watts for a typical 5" diameter wafer. The anode to cathode spacing between electrodes ranging from about 0.2 cm up to about 5 cm.

The silicon source may be a gaseous source such as silane (SiH_4) or a substituted silane such as, for example, SiH_2Cl_2. The source of oxygen may be N_2O or any other convenient and reasonably safe source of oxygen.

Typical flows of gas into a 5-10 liter d position chamber, using silan as th source of silicon and N_2O as the source of oxyg n, would be about 10-100 sccm of SiH_4 and about 100-5000 sccm N_2O. Under such d position conditions, a deposition rate of about 0.1 to about 2 µm/minute can be maintained until the desired thickness of conformal SiO_2 is achieved.

Silicon nitride may also be deposited instead of silicon oxide under the same high pressure deposition conditions by substituting a source of nitrogen for the source of oxygen. As in the low pressure process, nitrogen and (optionally) ammonia may be used as sources of nitrogen. Typical gas flows for deposition of silicon nitride, under the same conditions as for the high pressure deposition of silicon oxide, would be about 10 to about 100 sccm SiH_4, about 100 to about 10,000 sccm N_2, and about 0 to about 100 sccm NH_3 to achieve about the same deposition rate as for silicon oxide, i.e., from about 0.1 to about 2 µm/minute.

If it is desired to isotropically deposit a conformal layer of silicon oxynitride on a semiconductor wafer, a source of oxygen such as N_2O may be additionally supplied to the reactants used in forming silicon nitride, without substantially changing any other reaction conditions.

Thus, the invention provides an improved process for the etching and deposition of materials on a semiconductor wafer using a plasma energized by a power source operated at a frequency within a range of from about 50 MHz to about 800 MHz to provide a sheath voltage low enough to avoid risk of damage to devices on the wafer, yet high enough to achieve desired anisotropy, while permitting the process to be carried out at reaction rates comparable to prior art processes.

Claims

1. A process for fabricating integrated circuit devices on semiconductor wafers in a vacuum chamber containing an electrode upon which a semiconductor wafer is mounted which comprises maintaining a plasma in said chamber energized by one or more power sources connected to said electrode and operated within a frequency range of from 50 MHz to 800 MHz.

2. The process of claim 1, wherein said power source is operated at a power density ranging from 10 to 76 watts/inch^2 * of wafer area.

3. The process of claim 1 or 2, wherein process is carried out in combination with the use of auxiliary magnets arranged around the exterior of said chamber for magnetic enhancement.

* 1 inch^2 = 6.5 cm^2

4. The proc ss of one of the prec ding claims, wherein said plasma is elso coupled to another power source operated outside the frequency range of from 50 MHz to 800 MHz.

5. A plasma-assisted RIE process for etching materials used in the fabrication of integrated circuit devices on semiconductor wafers which comprises maintaining a plasma using a power source having a frequency range of from 50 MHz up to 800 MHz end maintained at a power density level ranging from 10 to 76 watts/inch^2 of wafer area in a vacuum etching chamber containing an anode and a wafer mounted on a cathode and maintained at a pressure within a range of from 2 to 500 milliTorr. **

6. The process of claim 5 wherein said anode end cathode electrodes heve e ratio of enode to cathode area of at least about 2:1 and an electrode spacing of about 5 cm or more.

7. The process of claim 5 or 6, wherein said anode and cathode electrodes have an electrode spacing ranging from 5 cm to 30 cm.

8. The process of one of claims 5 to 7, wherein said pressure in said chamber ranges from 20 to 200 milliTorr.

9. The process of one of claims 5 to 8, wherein said power density renges from 45 to 56 watts/inch^2 of wafer area.

10. The process of one of cleims 5 to 9 wherein said RIE process comprises a process for etching silicon oxide at an etch rate of from 0.3 to 0.75 µm/minute.

11. The process of claim 10, wherein said power source is operated within e frequency range of from 100 MHz to 250 MHz.

12. The process of one of cleims 5 to 1t, which further comprises flowing a source of fluorine, an optional source of hydrogen, a source of carbon, an optional source of oxygen, and an optional inert gas through said chamber while said plasma is ignited therein.

13. The process of claim 12 wherein said RIE process comprises a selective process for etching silicon oxide in preference to polysilicon or photoresist wher in the atomic ratio of carbon to fluorin ranges from 0.1:1 to 2:1 and the atomic ratio of hydrogen pres nt to fluorine ranges from 0.1:1 to 0.5:t to obtain e ratio ot silicon oxide etch (thickness) rate to polysilicon or photoresist etch (thickness) rate of from about 2:1 to over 30:t.

14. The process of one of claims 5 to 8 wherein said RIE process comprises a process for etching polysilicon and/or aluminum at an etch rate of from 0.2 to 1.0 µm/minute.

15. The process of claim 14 wherein said power source is operated within a frequency range of from 100 MHz to 800 MHz, preferably from 150 MHz to 600 MHz.

16. The process of cleim 14 or 15 wherein said power density ranges from 20 to 40 watts/inch^2 of wafer area.

17. The process of one of claims 14 to 16 which further comprises flowing a chlorine-containing gas and an optionel inert gas through seid chamber while said plasma is ignited therein.

18. A plasma-assisted high pressue process for etching materials used in the fabrication of integrated circuit devices on semiconductor wafers which comprises maintaining a plasma using one or more power sources having a frequency range of from 50 MHz up to 800 MHz and maintained at a power density level ranging from 15 to 76 watts/inch^2 of wafer area in a vacuum etching chamber containing an anode and a wafer mounted on a cathode and maintained at a pressure within a range of over 500 milliTorr to about 50 Torr.

19. The process of claim t8 wherein said enode and cathode electrodes have an electrode spacing of less than 5 cm, preferably ranging from 0.2 cm to 5 cm.

20. The process of claim 18 or 19 wherein said high pressure plesma etching process comprises a process for etching silicon oxide at an etch rate of from 0.2 to 1.0 µm/minute.

21. The process of claim 20 wherein said high pressure plasma etching process is operated within a pressure range of from 1 Torr to 20 Torr.

22. The process of claim 20 or 2t wherein the pow r is maintained at a power density level ranging from 30 to 50 watts/inch^2.

** 1 milliTorr = t.3x10' bars

23. The proc ss of one of claims 20 to 22 which further comprises flowing. a source of fluorina, a source of carbon, an optional source of hydrogen, and an optional inert gas through said chamber during said etch.

24. The process of one of claims 20 to 23 wherein said high pressure plasma process comprises a selectiva process for etching silicon oxide in preference to polysilicon or photoresist wherein the atomic ratio ot carbon to fluorine ranges from 0.1:1 to 2:1 and the atomic ratio of hydrogen present to fluorine ranges from 0.1:1 to 0.5:1 to obtain a ratio of silicon oxide etch (thickness) rate to polysilicon or photoresist etch (thickness) rate of from about 2:1 to over 30:1.

25. The process of claim 18 or 19 wherein said high prassure plasma etching process comprises a process for etching polysilicon and/or aluminum at an etch rate of from 0.2 to 1.0 µm/minute.

26. The process of claim 25 wherein said high pressure plasma etching process is operated within a pressure ranga of from 1 Torr to 20 Torr.

27. Tha process of claim 25 or 26 wharein the power is maintained at a power density level ranging from 20 to 40 watts/inch^2.

28. The process of one of claims 25 to 27 which further comprises flowing a source of chlorine and an optlonal Inert gas through said chamber during said etch.

29. A plasma-assisted low pressure CVD process for depositing matarials used in the fabrication of integrated circuit devices on semiconductor wafers which comprises maintaining a plasma using one or more power sources having a frequency range of from 50 MHz up to 800 MHz and maintained at a powar density leval ranging from 10 to 76 watts/inch^2 of wafer area in a vacuum deposition chamber containing an anode and a wafar mounted on a cathode and maintained at a pressure within a range of from 2 to 500 milliTorr.

30. The process of claim 29 wherein said anode and cathode electrodes have an anode to cathode electrode spacing of about 5 cm or more, pr ferably ranging from 5 cm to 30 cm.

31. The process of claim 29 or 30 wharein said low pressure CVD process comprises a proc ss for depositing silicon oxid at a d position rate of from 0.1 to 1.5 µm/minute.

32. The process of claim 31 wherain said power source is operated within a frequency range of from 100 MHz to 250 MHz.

33. The process of claim 31 or 32 wherain said pressure in said chamber ranges from 20 to 200 milliTorr.

34. The process of one of claims 31 to 33 wherein said power density ranges from 45 to 56 watts/inch^2 of wafar araa.

35. The process of one of claims 31 to 34 which further comprises flowing one or more sources of silicon, one or more sources of oxygen, and an optional inert gas through said chamber whila said plasma is ignitad therein.

36. The process of claim 29 or 30 wherein said low prassure CVD process comprises a process for depositing silicon nitride at a deposition rate of from 0.1 to 1.5 µm/minute.

37. Tha process of claim 36 wherein said power source is operated within a frequency range of from 100 MHz to 250 MHz.

38. The process of claim 36 or 37 wherein said pressure in said chamber ranges from 2 to 500 milliTorr, praferably from 20 to 200 milliTorr.

39. The process of one of claims 36 to 38 wherein sald power density ranges from 30 to 76 watts/inch^2 of wafer araa, preferably from 45 to 56 watts/inch^2 of wafer area.

40. The process of one of claims 36 to 39 which further comprises flowing one or more sources of silicon, one or more sources of nitrogen, an optional source of hydrogen, and an optional inert gas through said chamber while said plasma is ignited thara.

41. A plasma-assisted high pressura CVD conformal isotropic process for depositing materials used in the fabrication of integrated circuit devices on semiconductor wafers which comprises maintaining a plasma using ona or more power sources having a frequency range of from 50 MHz up to 800 MHz and maintained at a power density leval ranging from 10 to 38 watts/inch^2 of wafer area in a vacuum tching chamber containing an anode and a wafer mounted on a cathoda and maintained at a pressur within a range of over 500 milliTorr to

about 50 Torr.

42. The process of claim 41 wherein said anode and cathode electrodes have an anode to cathode electrode spacing of less than 5 cm, preferably ranging from 0.2 cm to 5 cm.

43. The process of claim 41 or 42 wherein said plasma-assisted high pressure conformal isotropic deposition process comprises a process for depositing silicon oxide at a deposition rate of from 0.5 to 1.0μm/minute.

44. The process of one of claims 41 to 43 wherein said process further comprises flowing one or more sources of silicon, one or more sources of oxygen, and an optional inert gas through the chamber.

45. The process of claim 44 which further comprises maintaining a pressure in said chamber ranging from 1 Torr to 20 Torr.

46. The process of one of claims 41 or 42 wherein said plasma-assisted high pressure conformal isotropic deposition process comprises a process for depositing silicon nitride at a deposition rate of from 0.5 to 1.0 μm/minute.

47. The process of claim 46 wherein said process further comprises flowing one or more sources of silicon, one or more sources of nitrogen, an optional source of hydrogen, and an optional inert gas through the chamber.

48. The process of claim 46 or 47 which further comprises maintaining a pressure in said chamber ranging from 1 Torr to 20 Torr.

PROVIDING A CHAMBER AT A PRESSURE OF FROM ABOUT 2 TO ABOUT 500 MILLITORR * CONTAINING AN ANODE AND A CATHODE, ON WHICH A SEMICONDUCTOR WAFER IS MOUNTED, WITH AN ELECTRODE SPACING OF 5 CM OR MORE

ETCHING A MATERIAL ON THE SEMICONDUCTOR WAFER USING A PLASMA ENERGIZED BY A POWER SOURCE OPERATED AT A FREQUENCY OF FROM ABOUT 50 MHz TO ABOUT 800 MHz AND A POWER DENSITY OF 10 TO 76 WATTS/IN^2 **

FIGURE 1

*1 milli Torr = $1,3 \times 10^{-6}$ bar

** 1 inch^2 = 6.5 cm^2

PROVIDING A CHAMBER AT A PRESSURE OF FROM ABOVE 500 MILLITORR TO ABOUT 50 TORR CONTAINING AN ANODE AND A CATHODE, ON WHICH A SEMICONDUCTOR WAFER IS MOUNTED, WITH AN ELECTRODE SPACING LESS THAN 5 CM

ETCHING A MATERIAL ON THE SEMICONDUCTOR WAFER USING A PLASMA ENERGIZED BY A POWER SOURCE OPERATED AT A FREQUENCY OF FRCM ABOUT 50 MHz TO ABOUT 800 MHz AND A POWER DENSITY OF 15 TO 76 WATTS/IN^2

FIGURE 2

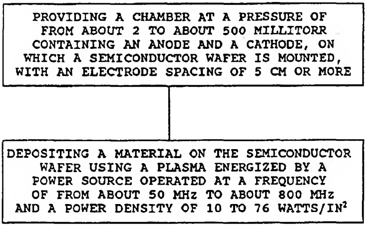
PROVIDING A CHAMBER AT A PRESSURE OF FROM ABOUT 2 TO ABOUT 500 MILLITORR CONTAINING AN ANODE AND A CATHODE, ON WHICH A SEMICONDUCTOR WAFER IS MOUNTED, WITH AN ELECTRODE SPACING OF 5 CM OR MORE
DEPOSITING A MATERIAL ON THE SEMICONDUCTOR WAFER USING A PLASMA ENERGIZED BY A POWER SOURCE OPERATED AT A FREQUENCY OF FROM ABOUT 50 MHz TO ABOUT 800 MHz AND A POWER DENSITY OF 10 TO 76 WATTS/IN²

FIGURE 3

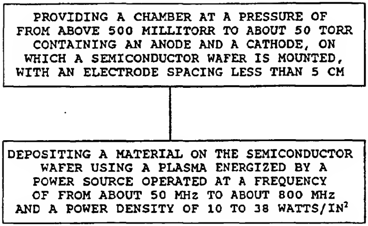
PROVIDING A CHAMBER AT A PRESSURE OF FROM ABOVE 500 MILLITORR TO ABOUT 50 TORR CONTAINING AN ANODE AND A CATHODE, ON WHICH A SEMICONDUCTOR WAFER IS MOUNTED, WITH AN ELECTRODE SPACING LESS THAN 5 CM
DEPOSITING A MATERIAL ON THE SEMICONDUCTOR WAFER USING A PLASMA ENERGIZED BY A POWER SOURCE OPERATED AT A FREQUENCY OF FROM ABOUT 50 MHz TO ABOUT 800 MHz AND A POWER DENSITY OF 10 TO 38 WATTS/IN^2

FIGURE 4